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Appl. No. 09/420,887
Amdt. dated 08/27/2004
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Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended):

A memory translation hub comprising:

- a memory bus interface that provides a memory bus having a memory bus cycle time;
- a memory channel interface that receives a memory control packet from a memory channel that times transmission of the memory control packet based on the memory bus cycle time, wherein the memory control packet includes command flag bits that indicate that the memory control packet is one of an activate command, a read/write command, and an extended command, the command flag bits being the first bits in the memory control packet; and
- a command generator coupled to the memory channel interface and to the memory bus interface, the command generator causing the memory bus interface to provide memory control signals on the memory bus responsive to the memory control packet.

2. (original):

The memory translation hub of claim 1 wherein the memory channel includes a control portion and a data portion, the memory channel interface receiving a memory control packet only from the control portion of the memory channel.

3. (cancelled)

4. (original):

The memory translation hub of claim 3 wherein the memory control packet specifies a memory row, a memory row address, a memory bank address, and a device identification mask if the memory control packet is the activate command.

5. (original):

The memory translation hub of claim 3 wherein the memory control packet specifies a memory row, a memory column address, and a memory bank address, if the memory control packet is the read/write command.

6. (original):

The memory translation hub of claim 3 wherein, if the memory control packet is the extended command, the memory control packet includes extended flag bits that indicate that the memory control packet is one of a retire with mask command, a pre-charge command, and a service command.